transistor load and with a standard MOS transistor load, respectively. Fig. 7B is the small signal transconductance variance due to ± 100 mV VSB using a standard MOS arrangement, whereas Fig. 7A is GM variance using the native MOS transistor. It is noted that the native MOS transistor provides a variance of ± 0.3% up to 1 MHz, whereas the standard MOS transistor has a variance of ± 9.7% over the same frequency range.--

IN THE CLAIMS:

Rewrite claims 1 and 7 as follows:

1. (Amended) A transconductance cell for use in a telecommunications receiver system on chip to reduce adverse effects of bulk semiconductor voltages on transconductance comprising a plurality of current sources interconnected to provide an output transconductance control voltage, and a variable load for the current sources including first and second load resistors each serially connected with one of the plurality of current sources, and a variable resistance interconnecting nodes of the load resistors, the variable resistance comprising a pair of native MOS transistors having low threshold voltages.

7. (Amended) The transconductance cell as defined by claim 4 wherein the system on a chip comprises a radio receiver, and the transconductance cell is used in a voltage controlled oscillator.

REMARKS

Claims 1-17 remain in the application with claim 7 amended to improve form.

Reconsideration is respectfully requested for claims 1-17.

The Examiner has noted that Figs. 3A-4 should be designated by a legend such as --prior art--. Enclosed is a copy of Figs. 3A-4 in which the legend--prior art--is added. Additionally, a Fig. 9 is added in which native transistors are shown